AMENDMENTS TO THE ABSTRACT:

Please delete the abstract and insert the attached substitute abstract after the claims.

An asynchronous FIFO apparatus includes a main FIFO memory, operable to store the data to be passed between the first and second clock domains, accessible from each clock domain under the control of an access pointer associated with that clock domain. For one or both of the clock domains, the amount of data accessible per clock cycle is variable. An auxiliary FIFO memory is associated with each clock domain in which the amount of data accessible per clock cycle is variable, and operable to store the access pointer used to access the main FIFO memory from its associated clock domain, and the access pointer being stored at a location of the auxiliary FIFO memory specified by an auxiliary access pointer. Routing logic passes the auxiliary access pointer to the other clock domain to enable that other clock domain to retrieve the access pointer stored in the auxiliary FIFO memory.